

MONDAY, MAY 15, 1961

SESSION 2: PARAMETRIC DEVICES

2:00 PM - 4:45 PM

CHAIRMAN: W. W. MUMFORD
BELL TELEPHONE LAB
WHIPPANY, NEW JERSEY

2.6

PASSIVE PHASE-DISTORTIONLESS PARAMETRIC LIMITERS

A. E. Siegman and I. T. Ho
Stanford University,
California

This paper presents theoretical and experimental results on a type of limiting action occurring in parametric circuits.¹ Let a signal at frequency ω be passed through a resonant tank at this frequency which is coupled by a nonlinear element to a resonant tank at the half frequency $\omega/2$. Above a certain threshold, the signal transmission through the ω tank will suddenly and sharply limit, in part because some of its energy goes into subharmonic $\omega/2$ oscillations, in part because the input VSWR to the device increases. This limiting principle can be implemented with varactor diodes or other parametric elements; it also explains the operation of previously known ferrite types of limiters.

The equivalent circuit of Fig. 1 has been analyzed to determine the steady-state and transient characteristics of such limiters. The steady-state analysis yields detailed design information for varactor diode limiters, in terms of the varactor diode characteristics. The transient solutions to the equations explain the leakage spikes observed in limiters of this type, particularly in ferrite versions, and to a lesser extent in varactor diode versions. The limiting action cannot begin until the subharmonic oscillations have built up from thermal noise. The larger the input compared to the threshold the faster this buildup. Therefore, as the input power is increased above the threshold level, the leakage spikes become shorter and higher, in the fashion shown in Fig. 2.

This description is modified when the rise time of the input pulse is comparable to the leakage spike length. The leakage spike then does not reach full height, because the subharmonic oscillations have time to build up while the input pulse rises. Figure 3 shows how the leakage spike peak amplitude 'saturates' at larger power levels when the input pulse has a finite rise time.

Several experimental varactor diode limiters have been tested at Stanford and elsewhere.^{2,3} An early S-band wave-

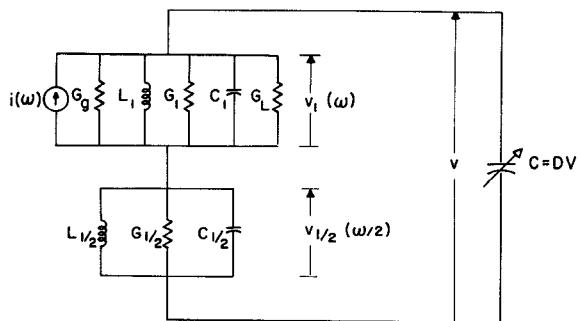
guide version used three diodes in parallel, shunted across a waveguide. The $\omega/2$ resonance came from the diodes resonating with the reactive characteristic impedance of the guide below cutoff. There was no ω resonance. Sharp limiting occurred over at least a 16 db range, with a 10/mw input threshold level, and less than 3° of phase shift over the entire range. Below-threshold insertion loss was ~10 db. A 126 Mc/s version using lumped circuits was used to observe the leakage spikes, which are too short to be readily seen in higher-frequency limiters. The most recent versions is a stripline limiter at S band, using a pill-type varactor diode. Figure 4 shows the construction of this limiter, and the mode patterns at the signal and subharmonic frequencies. Essentially flat limiting over at least a 20 db dynamic range above the threshold level of 1 milliwatt has been observed, as shown in Fig. 5. The insertion loss is ~ 4 db. The phase distortion has not yet been measured.

With further improvements in both varactor diodes and experimental circuits, still better limiter performance should be possible. This method of limiting appears to offer a simple method of obtaining sharp limiting at low-power levels with small phase distortion.

¹A. E. Siegman, "Phase-distortionless Limiting by a Parametric Method," Proc. IRE, Vol. 47, pp. 447-448; March 1959.

²A. D. Sutherland and D. E. Countiss, "Parametric Phase Distortionless L-band Limiter," Proc. IRE, Vol. 48, pp. 938; May 1960.

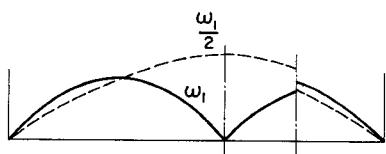
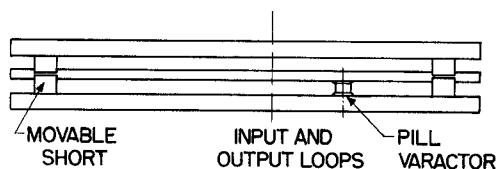
³A. A. Wolf and J. E. Pippin, "A Passive Parametric Limiter," 1960, Internat. Solid State Circuits Conf. Digest of Technical Papers, pp. 90-91; February 1960.



CIRCUIT MODEL

PASSIVE PARAMETRIC LIMITER

Figure 1 - Circuit Model of the Passive Parametric Limiter.



ELECTRIC FIELD DISTRIBUTION

STRIPLINE LIMITER

Figure 4 - Construction and Field Distribution of a Stripline Limiter.

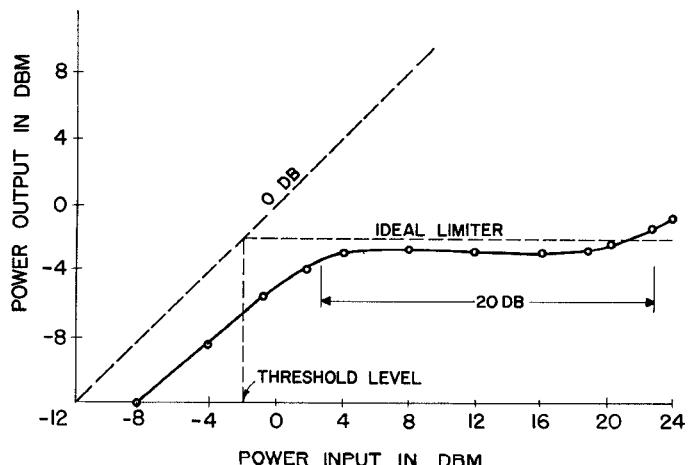


Figure 5 - Limiting Characteristic of the Stripline Limiter.

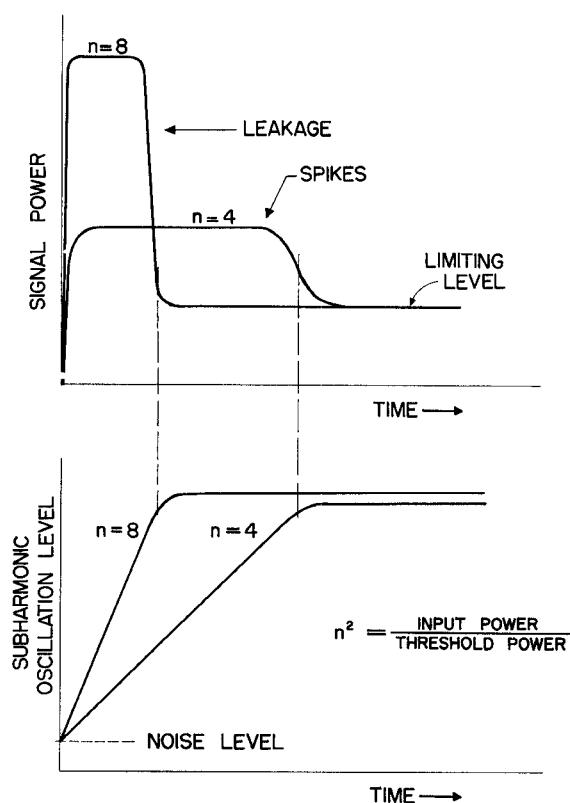


Figure 2 - Leakage Spikes for Various Input Power Levels.

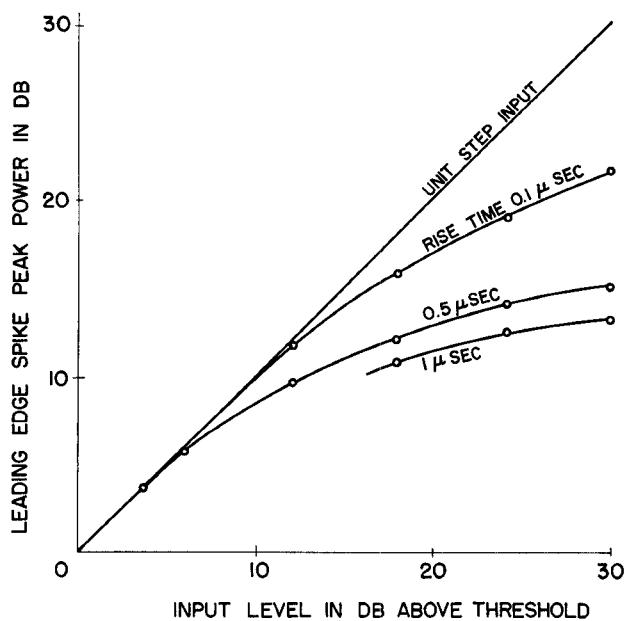


Figure 3 - Leakage Spike Amplitude vs Input Power for Various Rise Times.